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Automotive Discrete Group (ADG)
Power Transistor Division

Process Change Information

IRF630 and STD7NS20T4 Capacity extension in ST’s AMK Wafer Fab

Dear Customer,

Following the continuous improvement of our service and in order to increase productivity, we are pleased to announce that the product IRF630 and STD7NS20T4 currently manufactured in Catania will be also produced in ST’s AMK (Singapore) Wafer Fab.
The wafers, and the final assembled products, guarantee the same quality and electrical characteristics as current production.

In the next pages, we are reporting the qualification plan to reach full maturity.

The change has been classified as **Class 1** according to the ZVEI and ST internal rules.

	Assessment of impact on Supply Chain regarding following aspects - contractual agreements - technical interface of processability/manufacturability of customer - form, fit, function, quality performance, reliability	**Remaining risks on Supply Chain?**	
ID	**Type of change**	**No**	**Yes**
SEM-PW-13	Move of all or part of wafer fab to a different location/site/subcontractor	**P**	**P**

The qualification has been completed successfully in week 28/2018.

Sincerely Yours!

<table>
<tr><th colspan="2">IRF630 and STD7NS20T4 Capacity extension in ST’s AMK Wafer Fab</th></tr>
<tr><td>ST Part number:</td><td>ST PN: IRF630, STD7NS20T4
Package: TO220, DPAK</td></tr>
<tr><td>Reason and background of the change</td><td>To increase flexibility by improving capacity avoiding the risk for the customer to line down due to lack of silicon at FE level.</td></tr>
<tr><td>Detailed description of change(s), including affected type of changes</td><td>The Diffusion Process and Wafer Testing for IRF630 and STD7NS20T4 will be performed also in ST’s AMK (Singapore) Wafer Fab.</td></tr>
<tr><td>Impact on form, fit, function, or reliability.</td><td>No Impact</td></tr>
<tr><td>Datasheet</td><td>No Impact</td></tr>
<tr><td>Benefit of the change</td><td>Capacity and flexibility increase.</td></tr>
<tr><td>Planned Implementation date for change</td><td>The qualification has been completed according to the following plan:
<table>
<tr><th>Test Vehicles</th><th>N. of Lots</th><th>Type of verification</th><th>Forecast</th></tr>
<tr><td>IRF630</td><td>1</td><td rowspan="3">Complete</td><td rowspan="3">Completed</td></tr>
<tr><td>STD7NS20T4</td><td>1</td></tr>
<tr><td>Family Data</td><td>3</td></tr>
</table>
Forecast for Samples Availability → wk 28/2018
Forecast for Qualification release → Done
Forecast for Start of Production → begin of Q4/2018</td></tr>
</table>

IRF630 and STD7NS20T4 products
Capacity extension in ST's AMK Wafer Fab
Product transfer
(Industrial)

General Information	
Commercial Product	_:IRF630_ _:STD7NS20T4_
Product Line (Test Vehicle)	_: MM21_
Product Description	_: Power MOSFET_
Package	_: TO 220_ _: DPAK_
Silicon Technology	: MESH OVERLAY™
Division	_: Power Transistor Division_

Traceability	
Diffusion Plant	: SG6" _(Singapore_)
Assembly Plant	_: TO-220: Bouskoura (Morocco)_ _:DPAK: Shenzhen (China)_

Reliability Assessment	
Passed	☒

**Disclaimer:** this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)

REVISION HISTORY

Version	Date	Author	Changes description
1.0	11-July-2018	A.SETTINIERI	Final Report

APPROVED BY:
Corrado CAPPELLO
ADG Q&R department - Catania
ST Microelectronics

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1. RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Reliability evaluation for IRF630 and STD7NS20T4 products capacity extension in ST's AMK Wafer Fab

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with JESD47 and internal spec 0061692 specification and are listed in the Test Plan.
For details on test conditions, generic data used and spec reference see test results summary at Par.3

#	Stress	Abrv	Reference	Test Flag	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	Y	
2	External Visual	EV	JESD22B-101	Y	
3	High Temperature Reverse Bias	HTRB	JESD22A-108	Y	
4	High Temperature Gate Bias	HTGB	JESD22A-108	Y	
5	Pre-conditioning	PC	JESD22A-113	Y	
6	High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	Y	
7	Temperature Cycling	TC	JESD22A-104	Y	
8	Autoclave	AC	JESD22A-102	Y	
9	Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	Y	

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die and package oriented test showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.

On the basis of the overall results obtained, we can give a positive judgment on the reliability evaluation for IRF630 and STD7NS20T4 products capacity extension in SG6" (Singapore) Wafer Fab in agreement with JESD47 and 0061692 internal specification.

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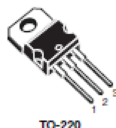
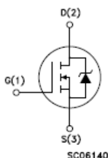
2. DEVICE/TEST VEHICLE CHARACTERISTICS

2.1 Pin connection





2.2 Traceability

Reference “Product Baseline” document if existing, else provide following chapters/information:

D.U.T.: IRF630 PACKAGE: TO-220

Wafer fab information	
Wafer fab manufacturing location	Singapore
Wafer diameter (inches)	6”
Silicon process technology	MESH OVERLAY™
Die finishing front side (passivation)	No Passivation
Die finishing back side	Ti-Ni-Ag
Die area (Stepping die size)	2280x2160 μm²
Metal levels/Materials	Al/Cu

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Mororcco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220
Die attach material	Preform Pb /Ag/Sn
Wires bonding materials/diameters	Gate :Al 5mils ; Source: Al 10 mils
Molding compound	Halogeen Free molding compound

D.U.T.: STD7NS20T4 PACKAGE: DPAK

Wafer fab information	
Wafer fab manufacturing location	Singapore
Wafer diameter (inches)	6”
Silicon process technology	MESH OVERLAY™
Die finishing front side (passivation)	No Passivation
Die finishing back side	Ti-Ni-Ag
Die area (Stepping die size)	2280x2160 μm²
Metal levels/Materials	Al/Cu

Assembly information

Assembly Information	
Assembly plant location	Shenzhen (China)
Package code description	DPAK
Leadframe/Substrate	FRAME TO252
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate :Al 5mils ; Source: Al 10 mils
Molding compound	Halogeen Free molding compound

Reliability testing information

Reliability Testing Information	
Reliability laboratory location	Catania (Italy)
Electrical testing location	Catania (Italy)
Tester	Tesec

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3. TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	**Commercial Product**	**Product lines**	**Package**	**Wafer Fab**	**Assembly plant**	**Note**
1	IRF630 -	MM2101	TO-220	SG6” (Singapore)	Bousckoura (Morocco)	
2	STD7NS20T4		DPAK		Shenzhen (China)	
Product / Technology Family data						
3	STP60NF10	MM0H	TO-220	SG6” (Singapore)	Shenzhen (China)	
4	STD10NF30	MM3E	DPAK			
5	STB18NF30	MM3H	D2PAK			

3.2 Test results summary

Test plan results are summarized in the following template.

#	**Stress (Abrv)**	**PC**	**Std ref.**	**Conditions**	**Sample Size (S.S)**	**Steps**	**Failure/SS**				
							Lot 1	**Lot 2**	**Lot 3**	**Lot 4**	**Lot 5**
									Technology/Product Family data		
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			90	190	190	190	190
2	**External visual**		JESD22 B-101	All devices submitted for testing			90	190	190	190	190
Silicon Oriented Tests											
4	**HTRB**	N	JESD22 A-108	Tj=175°C ; BIAS= 160V	90	1000H	0/45	0/45			
				Tj=175°C ; BIAS= 80V	45				0/45		
				Tj=175°C ; BIAS= 240V	90					0/45	0/45
5	**HTGB**	N	JESD22 A-108	Tj=175°C ; BIAS= 20V	225	1000H	0/45	0/45	0/45	0/45	0/45
Package Oriented Tests											
6	**Pre-conditioning**		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C,RH=85% IR Reflow @ 260°C 3 times	All devices to be subjected to H3TRB, TC,AC,IOL	Final		Pass		Pass	Pass
7	**H3TRB**	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS= 100V	100	1000H		0/25	0/25	0/25	0/25
8	**AC**	Y	JESD22 A-102	Ta=121°C , P=2atm	100	96H		0/25	0/25	0/25	0/25
9	**TC**	Y	JESD22 A-103	Ta= – 65°C / +150°C	100	500cy		0/25	0/25	0/25	0/25
10	**IOL/TF**	Y	MIL-STD-750 Method 1037	ΔTj≥100°C	100	10Kcy		0/25	0/25	0/25	0/25

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